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IMPROVED ECP GAP FILL BY MODULATING THE VOLTAGE ON THE SEED LAYER TO INCREASE CUT CONCENTRATION INSIDE FEATURE

INVENTORS:

BO ZHENG
RENREN HE
GIRISH DIXIT

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Beth Mulcahy
Signature

BETH MULCAHY
Name

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BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention generally relates to electroplating processes for sub-quarter micron semiconductor devices. More particularly, the present invention relates to electroplating copper into vias of sub-quarter micron semiconductor devices.

Description of the Related Art

[0002] Sub-quarter micron multi-level metallization is one of the key technologies for the next generation of ultra large scale integration (ULSI). The multilevel interconnects that lie at the heart of this technology require planarization of interconnect features formed in high aspect ratio apertures, including contacts, vias, lines, and other features. Reliable formation of these interconnect features is critical to the success of ULSI and to the continued effort to reliably increase circuit density on individual substrates and die.

[0003] As circuit density increases, the widths of vias, contacts, and other features, as well as the width of the dielectric materials positioned therebetween, decreases to less than 250 nanometers, while the thickness of the dielectric layers themselves remains substantially constant. This results in the aspect ratios for the features, *i.e.*, their height divided by width, increasing, often well over 4:1. However, many traditional deposition processes, such as physical vapor deposition (PVD) and chemical vapor deposition (CVD), for example, are known to have difficulty filling high aspect ratio features and structures, particularly when the aspect ratio exceeds 10:1. Therefore, there is a great amount of ongoing effort being directed toward the formation of void-free, nanometer-sized features having high aspect ratios, *i.e.*, 4:1 or higher. Additionally, as the feature width decreases, the device electrical current generally remains constant or increases, which results in an increased current density in the feature.

[0004] Elemental aluminum (Al) and several of it's alloys have been the traditional metals used to form lines and plugs in semiconductor processing as a result of aluminum's perceived low electrical resistivity, its superior adhesion to silicon dioxide (SiO_2), its ease of patterning, and the availability of aluminum in a relatively pure form. Tungsten and it's alloys have also been a conventional choice for line and plug formation as a result of the resistivity exhibited therefrom. However, aluminum and tungsten both have higher electrical resistivities than other more conductive metals, such as copper, for example, and further, aluminum and tungsten typically offer poor resistance to electromigration.

[0005] Copper and its alloys appear to be promising replacements for conventional aluminum and tungsten based processes, as copper generally exhibits lower resistivity than aluminum and tungsten, while also offering significantly higher electromigration resistances than aluminum and tungsten. These characteristics are important for supporting the higher current densities experienced at high levels of integration and increased device speed. Additionally, copper also exhibits favorable thermal conductivity and is readily available in a relatively pure state. Therefore, copper is generally becoming a choice metal for filling sub-quarter micron high aspect ratio interconnect features on semiconductor substrates.

[0006] Aside from the desirability for using copper in semiconductor device fabrication, effective fabrication methods for depositing copper into very high aspect ratio features, such as a 4:1 or higher having 0.35μ (or less) wide vias are limited, as known deposition techniques, such as PVD and CVD, are generally not effective in completely filling these small vias in copper based systems. Therefore, in order to facilitate the use of copper in semiconductor device fabrication, electroplating processes, which have previously been limited to the fabrication of lines and/or bump solder points, are now being investigated as possible processes for filling vias and contacts on sub-quarter micron semiconductor devices.

[0007] Metal electroplating processes are generally known, and may be achieved through a variety of techniques. A typical electroplating method used to manufacture semiconductor devices generally includes using either a CVD or a PVD

process to deposit a barrier layer over feature surfaces, using another CVD or PVD process to deposit a conductive metal seed layer over the barrier layer, which is preferably copper, and then electroplating a conductive metal layer over the seed layer to fill the structure/feature. Finally, the deposited layers may then be planarized, through, for example, a chemical mechanical polishing (CMP) process, to remove the overburden and reveal the properly defined and filled conductive interconnect feature.

[0008] When copper is used as the conductive material in the electroplating process, a lower resistivity is shown and destructive cross talk is generally reduced. However, the process of electroplating copper into and filling sub-quarter micron vias through conventional electroplating processes has been shown to be unsuccessful, as the limited dimensions of sub-quarter micron vias generally does not allow for sufficient electrolyte flow into and out of the vias to support sustained electroplating. For example, when an electroplating process is used to fill a sub-quarter micron via, the surface containing the via is generally exposed to a flow of electrolyte having the plating material therein. A constant electrical bias is then applied between the electrolyte and the surface to be plated (seed layer), which acts to bias or pull the plating material (ions) from the electrolyte and plate/deposit the ions on the plating surface. However, the plating process depletes plating ions from the electrolyte, and therefore, it is generally necessary to supply fresh electrolyte to the plating surface in order to provide a continual supply of ions to be plated. The supply of fresh electrolyte to flat surfaces to be plated is easily accomplished. However, when it comes to sub-quarter micron vias, it is generally not possible to flow electrolyte into the ion depleted regions of vias as a result of the limited dimensions of the via itself. Therefore, the plating ions must generally diffuse from areas of high ion concentration within the electrolyte outside the vias into areas of lower ion concentration inside the vias in order for the via to be plated or filled. The plating ions are generally caused to diffuse into the vias by the constant electrical plating bias applied between the substrate and the electrolyte, which operates to urge plating ions to diffuse through the electrolyte to areas of lower ion concentration within the electrolyte. Dynamic fluid diffusion principles are the general cause for

the diffusion of the plating ions through the electrolyte to areas of low ion concentration. However, fluid diffusion of plating ions from one concentration to another in conventional plating systems is extremely slow and generally impracticable for semiconductor plating processes. Additionally, the diffusion of plating ions as a result of the electrical plating bias is known to be a slow process, as well as potentially causing closure of the vias prior to filling.

[0009] Therefore, in view of the deficiencies of conventional plating apparatuses and processes for sub-quarter micron vias, there is a need for a plating apparatus and method capable of accelerating diffusion of plating ions into vias of sub-quarter micron devices. Further, there is a need for a plating apparatus and method capable of accelerating diffusion of plating ions into vias while avoiding closure prior to completely filling the via.

SUMMARY OF THE INVENTION

[0010] Embodiments of the invention generally provide a processing cell for an electro-chemical deposition system. The processing cell includes a head assembly configured to support a wafer, the head assembly including a cathode, and an electrolyte container configured to hold a fluid electrolyte therein and having an anode disposed within the container. The processing cell further includes a power supply in electrical communication with the cathode and the anode, the power supply being configured provide a pulsed power waveform to the cathode and anode.

[0011] Embodiments of the invention further provide an apparatus for electro-chemically depositing a metal onto a substrate. The apparatus generally includes a head assembly having a cathode and a wafer holder disposed above the cathode. The apparatus further includes a process kit disposed below the head assembly, the process kit including an electrolyte container configured to receive and maintain a fluid electrolyte therein, and an anode disposed in the electrolyte container. The apparatus further includes a power supply in electrical communication with the cathode and the anode, the power supply being configured to provide a varying amplitude electrical signal to the anode and cathode.

[0012] Embodiments of the invention further provide a method for electroplating metal into sub-quarter micron integrated circuit features. The method includes providing an electrolyte container configured to receive and maintain a fluid electrolyte therein, the electrolyte container having an anode disposed within the electrolyte container. The method further includes providing a head assembly positioned above the electrolyte container, the head assembly including a wafer holder for supporting a wafer and a cathode. The method further includes positioning a wafer in the electrolyte container in contact with the fluid electrolyte, and applying a varying amplitude waveform to the cathode and anode in an electroplating process.

[0013] Embodiments of the invention further provide a method for electroplating metal including the steps of providing an electrolyte having an anode disposed therein, providing a cathode in electrical communication with a wafer to be plated, and applying a varying amplitude voltage waveform to the cathode and anode in a plating process.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] So that the manner in which the above recited features, advantages and objects of the present invention are attained and can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to the embodiments thereof which are illustrated in the appended drawings.

[0015] It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0016] Figure 1 illustrates a perspective view of an electroplating system of the invention.

[0017] Figure 2 illustrates a plan view of an electroplating system of the invention.

[0018] Figure 3 illustrates a sectional view of an electroplating cell of the invention.

[0019] Figure 4 illustrates three-dimensional partial sectional view of a cathode contact ring of the invention.

[0020] Figure 5 illustrates an exemplary time/voltage plot for an electroplating voltage of an embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0021] Figure 1 is a perspective view of an electroplating system platform 100 of the invention. Figure 2 is a schematic view of the electroplating system platform 100 of the invention. Referring cooperatively to both Figures 1 and 2, the electroplating system platform 100 generally includes a loading station 110, a thermal anneal chamber 111, a spin-rinse-dry (SRD) station 112, a mainframe 114, and an electrolyte replenishing system 120. Preferably, the electroplating system platform 100 is enclosed in a clean room-type environment using, for example, plexiglass panels. The mainframe 114 generally includes a mainframe transfer station 116 and a plurality of processing stations 118. Each processing station 118 includes one or more processing cells 140. An electrolyte replenishing system 120 is positioned adjacent the electroplating system platform 100 and in fluid communication with process cells 140 in order to circulate electrolyte to cells 140 that will be used for the electroplating process. The electroplating system platform 100 also generally includes a control system 122, which may be a programmable microprocessor configured to interface with the various components of the system platform 100 and provide controlling signals thereto. Control system 122 may generally operate to control the cooperative operation of each of the components that together form system platform 100.

[0022] Loading station 110 generally includes one or more wafer cassette receiving areas 124, one or more loading station transfer robots 128, and at least one wafer orientor 130. The number of wafer cassette receiving areas 124, loading station transfer robots 128, and wafer orientors 130 included in the loading station 110 may be configured according to the desired throughput of the system. As shown for one exemplary embodiment in Figures 1 and 2, the loading station 110 includes two wafer cassette receiving areas 124, two loading station transfer robots 128, and one

wafer orientor 130. Wafer cassette 132 containing wafers 134 are loaded onto the wafer cassette receiving area 124 to introduce wafers 134 into the electroplating system platform 100. The loading station transfer robots 128 then transfer wafers 134 between the wafer cassette 132 and the wafer orientor 130. The wafer orientor 130 positions each wafer 134 in a desired orientation to ensure that the wafer 134 is properly processed. The loading station transfer robot 128 also transfers wafers 134 between the loading station 110 and the SRD station 112 and between the loading station 110 and the thermal anneal chamber 111.

[0023] Figure 3 is a cross sectional view of an electroplating process cell 300 according to the invention. The electroplating process cell 300 is similar to the electroplating process cell 140 as shown in Figures 1 and 2. The processing cell 300 generally includes a head assembly 310, a process kit 320 and an electrolyte collector 340. Preferably, the electrolyte collector 340 is secured onto the body 342 of the mainframe 114 over an opening 343 that defines the location for placement of the process kit 320. The electrolyte collector 340 includes an inner wall 346, an outer wall 348, and a bottom 347 connecting the respective walls. An electrolyte outlet 349 is disposed through the bottom 347 of the electrolyte collector 340 and connected to the electrolyte replenishing system 120 (shown in Figure 1) through tubes, hoses, pipes or other fluid transfer connectors. Process kit 320 also includes an anode positioned within the electrolyte collector 340 so that the anode is in electrical communication with the electrolyte. The anode may be encapsulated within a permeable encapsulation member configured to allow electrolyte flow therethrough, while preventing any plating material from traveling through the permeable encapsulation member.

[0024] The head assembly 310 is generally mounted onto a head assembly frame 352. The head assembly frame 352 includes a mounting post 354 and a cantilever arm 356. The mounting post 354 is mounted onto the body 342 of the mainframe 114, and the cantilever arm 356 extends laterally from an upper portion of the mounting post 354. Preferably, the mounting post 354 provides rotational movement with respect to a vertical axis along the mounting post to allow rotation of the head

assembly 310. The head assembly 310 is attached to a mounting plate 360 disposed at the distal end of the cantilever arm 356. The lower end of the cantilever arm 356 is connected to a cantilever arm actuator 357, such as a pneumatic cylinder, mounted on the mounting post 354. The cantilever arm actuator 357 provides pivotal movement of the cantilever arm 356 with respect to the joint between the cantilever arm 356 and the mounting post 354. When the cantilever arm actuator 357 is retracted, the cantilever arm 356 moves the head assembly 310 away from the process kit 320 to provide the spacing required to remove and/or replace the process kit 320 from the electroplating process cell 300. When the cantilever arm actuator 357 is extended, the cantilever arm 356 moves the head assembly 310 toward the process kit 320 to position the wafer in the head assembly 310 in a processing position.

[0025] The head assembly 310 generally includes a wafer holder assembly 350 and a wafer assembly actuator 358. The wafer assembly actuator 358 is mounted onto the mounting plate 360, and includes a head assembly shaft 362 extending downwardly through the mounting plate 360. The lower end of the head assembly shaft 362 is connected to the wafer holder assembly 350 to selectively position the wafer holder assembly 350 in either a processing position or a wafer loading position. The wafer holder assembly 350 generally includes a wafer holder 364 and a cathode contact ring 366, which is further illustrated in cross section in Figure 4 as contact ring 466. In general, contact ring 366 includes an annular body having a plurality of conducting members disposed thereon. The annular body is constructed of an insulating material to electrically isolate the plurality of conducting members. Together the body and conducting members form an interior substrate-seating surface, which during processing, supports a substrate and provides electrical communication thereto.

[0026] Figure 4 is a perspective view of an exemplary contact ring 466 of the invention having a partial sectional view thereof. Contact ring 466 generally includes a plurality of conducting members 465 at least partially disposed within an annular insulative body 470. The insulative body 470 includes a flange 462 and a downward

sloping shoulder portion 464 leading to a substrate seating surface 468 located below the flange 462 such that the flange 462 and the substrate seating surface 468 lie in offset and substantially parallel planes. Thus, the flange 462 may be understood to define a first plane while the substrate seating surface 468 defines a second plane parallel to the first plane, wherein the shoulder 464 is disposed between the two planes. However, the contact ring design shown in Figure 4 is intended to be merely illustrative, and therefore, various modifications may be made to ring 466 without departing from the scope of the invention. For example, in another embodiment, the shoulder portion 464 may be of a steeper angle including a substantially vertical angle so as to be substantially normal to both the flange 462 and the substrate seating surface 468. Alternatively, the contact ring 466 may be substantially planar thereby eliminating the shoulder portion 464.

[0027] The conducting members 465 of contact ring 466 are defined by a plurality of outer electrical contact pads 480 annularly disposed about flange 462, a plurality of inner electrical contact pads 472 radially disposed about the substrate seating surface 468, and a plurality of embedded conducting connectors 476 that link the pads 472, 480 to one another. The conducting members 465 are isolated from one another by the insulative body 470 that may be made of a plastic, such as polyvinylidenefluoride (PVDF), perfluoroalkoxy resin (PFA), Teflon™, and Tefzel™, or other insulating material such as Alumina (Al_2O_3) or other ceramics. The outer contact pads 480 are coupled to a power supply (not shown) in order to deliver current and voltage to the inner contact pads 472 via the connectors 476 during processing. In turn, the inner contact pads 472 supply the current and voltage to a substrate by maintaining contact around a peripheral portion of the substrate. Thus, in operation the conducting members 465 act as discrete current paths electrically connected to a substrate.

[0028] Low resistivity, and conversely, high conductivity, are directly related to good plating. To ensure low resistivity, conducting members 465 are preferably made of copper (Cu), platinum (Pt), tantalum (Ta), titanium (Ti), gold (Au), silver (Ag), stainless steel, or other conducting materials. Low resistivity and low contact

resistance may also be achieved by coating the conducting members 465 with a conducting material. Thus, the conducting members 465 may, for example, be made of copper (resistivity for copper is approximately 2×10^{-8} Ω·m) and be coated with platinum (resistivity for platinum is approximately 10.6×10^{-8} Ω·m). Coatings such as tantalum nitride (TaN), titanium nitride (TiN), rhodium (Rh), Au, Cu, or Ag on a conductive base materials such as stainless steel, molybdenum (Mo), Cu, and Ti are also possible. Additionally, coating the contacts may also operate to prevent plating on the contacts. Further, since the contact pads 472, 480 are typically separate units bonded to the conducting connectors 476, the contact pads 472, 480 may comprise one material, such as Cu, and the conducting members 465 another, such as stainless steel. Either or both of the pads 472, 180 and conducting connectors 476 may be coated with a conducting material. Additionally, because plating repeatability may be adversely affected by oxidation, which acts as an insulator, the inner contact pads 472 preferably comprise a material resistant to oxidation such as Pt, Ag, or Au.

[0029] Typically, one or more power supplies may be in communication with the outer contact pads 480 of the cathode contact ring 466, resulting in parallel circuits through the inner contact pads 472. The power supplies in communication with contact pads 480 will generally be power supplies configured to supply and precisely regulate the voltage and current applied to the contact pads 480. This control may be managed by a microprocessor in communication therewith, or alternatively, through other electronic devices configured to monitor and regulate the output power of the power supplies. Regulated and controlled power supplies is important, as the inner contact pad-to-substrate interface resistance will often vary between each inner contact pad 472. As a result thereof, more current will flow through contact pads 472 having lesser resistances, and therefore, more plating will occur proximate these particular contact pads 472 having lower resistances. However, by placing an external resistor in series with each conducting member 465, the value or quantity of electrical current passed through each conducting member 465 may be controlled by adjusting the value of the external resistor. This control process may be undertaken by the power supply controller, or alternatively, by a separate electronic

device configured to monitor and adjust the variable resistor in order to maintain a constant voltage and current through contacts pads 472. As a result of the control process of the invention, the variations in the electrical properties between each of the inner contact pads 472 do not affect the current distribution on the substrate, and a uniform current density results across the plating surface that contributes to a uniform plating thickness. The external variable resistors may also allow and provide for a uniform current distribution between different substrates of a process-sequence.

[0030] The following is a description of a typical wafer electroplating process sequence through the exemplary electroplating system platform 100 shown in Figure 1. A wafer cassette containing a plurality of wafers is loaded into the wafer cassette receiving area 124 in the loading station 110 of the electroplating system platform 100. A loading station transfer robot 128 picks up a wafer from a wafer slot in the wafer cassette and places the wafer on the wafer orientor 130. The wafer orientor 130 determines and orients the wafer to a desired orientation for processing through the system 100. The loading station transfer robot 128 then transfers the oriented wafer from the wafer orientor 130 and positions the wafer in one of the wafer slots in the wafer pass-through cassette 138 in the SRD station 112. The mainframe transfer robot 142 picks up the wafer from the wafer pass-through cassette 138 and positions the wafer for transfer by the flipper robot 148. The flipper robot 148 rotates its robot blade below the wafer and picks up wafer from mainframe transfer robot blade. A vacuum suction gripper on the flipper robot blade secures the wafer on the flipper robot blade, and the flipper robot flips the wafer from a face up position to a face down position. The flipper robot 148 rotates and positions the wafer face down in the wafer holder assembly 350. The wafer is positioned below the wafer holder 364 but above the cathode contact ring 466. The flipper robot 148 then releases the wafer to position the wafer into the cathode contact ring 466. The wafer holder 364 moves toward the wafer and the vacuum chuck secures the wafer on the wafer holder 364. A bladder assembly on the wafer holder assembly 450 exerts pressure against the wafer backside to ensure electrical contact between the wafer plating surface and the cathode contact ring 466.

[0031] The head assembly 452 is lowered to a processing position above the process kit 320. At this position the wafer is below the upper plane of a weir and contacts the electrolyte contained in the process kit 320. A power supply is activated to supply electrical power (*i.e.*, voltage and current) to the cathode and the anode to enable the electroplating process. The electrical power supplied is traditionally a constant voltage and current, and the electrolyte in the processing kit 320 is typically continually pumped into the process kit 320 during the electroplating process. The electrical power supplied to the cathode and anode and the flow of the electrolyte are controlled by a control system to achieve the desired electroplating results. The combination of the electrolyte, which is rich in plating ions, and a constant electrical bias being applied to the plating surface allows for the plating ions to be deposited/plated on the plating surface. Additionally, the head assembly may be rotated as the head assembly is lowered and also during the electroplating process.

[0032] After the electroplating process is completed, the head assembly 410 raises the wafer holder assembly 450 and removes the wafer from the electrolyte. Preferably, the head assembly 452 is rotated for a period of time to enhance removal of residual electrolyte from the wafer holder assembly 450. The vacuum chuck and the bladder assembly of the wafer holder then release the wafer from the wafer holder, and the wafer holder is raised to allow the flipper robot blade 148 to pick up the processed wafer from the cathode contact ring 466. The flipper robot 148 rotates the flipper robot blade above the backside of the processed wafer in the cathode contact ring 466 and picks up the wafer using the vacuum suction gripper on the flipper robot blade. The flipper robot 148 rotates the flipper robot blade with the wafer out of the wafer holder assembly, flips the wafer from a face-down position to a face-up position, and positions the wafer on the mainframe transfer robot blade. The mainframe transfer robot then transfers and positions the processed wafer above the SRD module 136 for drying. After drying, the loading station transfer robot 228 picks up the wafer from the SRD module 136 and transfers the processed wafer into the RTA chamber 111 for an anneal treatment process to enhance the properties of the deposited materials. The annealed wafer is then transferred out of

the RTA chamber 111 by the loading station robot 128 and placed back into the wafer cassette for removal from the electroplating system. The above-described sequence can be carried out for a plurality of wafers substantially simultaneously in the electroplating system platform 100 of the present invention. Also, the electroplating system according to the invention may be adapted to provide multi-stack wafer processing.

[0033] Embodiments of the invention improve upon conventional plating processes and apparatuses via application of a varied amplitude electrical bias waveform, *i.e.*, a pulsed or modulated electrical bias waveform, to the plating surface. More particularly, conventional power application processes generally apply a constant electrical bias to the plating surface in order to draw ions from the electrolyte to the plating surface. The pulsed or modulated bias, which may be pulsed in a square wave, saw tooth wave, sinusoidal wave, other waveforms having generally oscillatory type characteristics, or variations thereof, generally uses increased voltage magnitude on the positive/upper portions of the pulses in order to encourage diffusion of plating ions deep into sub-quarter micron features, while also using low magnitude voltage on the lower/negative portions of the pulses. The lower/negative portion of the power pulses operate to plate at lower current density for a period of time, which facilitates avoidance of plating closure of the top of the features. Therefore, the pulsed bias to the plating surface operates to both facilitate diffusion of plating ions into the lower portions of smaller features, while also avoiding close of the feature top opening from overplating.

[0034] Figure 5 illustrates an exemplary electroplating voltage bias application 500. The voltage bias application 500, although represented as a square wave in the current exemplary embodiment, is not limited to any specific waveform. Voltage bias 500 includes a sequence of large magnitude positive voltage bias portions 501 and low magnitude positive voltage bias portions 502. The high and low voltage portions are sequentially applied in an alternating sequence, *i.e.*, high, low, high, low, etc. The high voltage portions 501 may be, for example, in the range of about 5 volts to about 10 volts. Alternatively, the high voltage portions may be in the range

of about 2 volts to about 15 volts, for example, for a 200 millimeter substrate. The current density of the high voltage portions may be in the range of about 8 milliamps per square centimeter to about 50 milliamps per square centimeter. More particularly, the current density of the high voltage portions may be in the range of about 16 milliamps per square centimeter to about 32 milliamps per square centimeter. The low voltage portions 502 may be, for example, in the range of about .3 volts to about 1.5 volts. Alternatively, the low voltage portions may be between about 0 volts and about 2 volts. The duration of the high voltage pulse 501, which is represented by 503 in Figure 5, may be between about 50 milliseconds and about 500 milliseconds in duration, for example. The duration of the low voltage pulse 502, which is represented by 504 in Figure 5, may be between about 50 milliseconds and about 500 milliseconds, for example. Therefore, the combination of the high voltage pulse duration and high voltage magnitude may be calculated to maximize ion diffusion into sub-quarter micron features, as the high voltage parameters may be calculated to drive or attract plating ions into the vias for plating during the low voltage portions. The combination of the low voltage pulse duration and low voltage magnitude may be calculated to optimize plating in sub-quarter micron features without causing closure of the features prior to the feature being completely filled with plating material. The combination of the high and low voltage portions cooperatively operate to diffuse the maximum number of plating ions into the vias and to plate these ions without causing a top closure condition prior to completely filling the via. The present exemplary embodiment may sequentially apply the high and low voltage pulses to the surface to be plated for a predetermined number of cycles (a cycle equals one sequence of a high pulse followed by a low pulse), which may be between about 5 cycles and about 50 cycles.

[0035] In yet another exemplary embodiment of the invention, the bias voltage application may be modified to include a pulsed or modulated voltage sequence, wherein a sequence of large magnitude voltage portions and low magnitude negative voltage portions are applied to the plating surface. In this exemplary embodiment the large magnitude voltage portions may be in the range of about 2

volts to about 15 volts, and preferably in the range of about 5 volts to about 10 volts. The low voltage portions may be in the range of about negative .1 volts to about negative 2 volts, and preferably in the range of about negative .3 volts to about negative 1.5 volts. In this embodiment the high voltage portions are calculated to encourage electrolyte ion diffusion into the sub-quarter micron features. Additionally, the low voltage portions are calculated to facilitate void free gap fill by avoiding closure of sub-quarter micron features through slower plating during the lower voltage portions, however, the low voltage portions may be negative in the present exemplary embodiment, which may operate to substantially reduce and/or reverse the plating process in order to prevent voids in the gap fill.

[0036] While the foregoing is directed to embodiments of the present invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.